REMARKS

This Amendment responds to the Office Action mailed January 24, 2007 in the above-identified application. Based on the foregoing amendments and the following comments, reconsideration and allowance of the application are respectfully requested.

Claims 1-24 were previously pending in the application. No claims have been amended. Claims 9-24 have been withdrawn from consideration and are canceled without prejudice or disclaimer. Applicant expressly reserves the right to file the withdrawn claims in one or more divisional applications. New claims 25-27 have been added. The new claims find clear support in the original application at least at page 10, line 10 to page 11, line 2. No new matter has been added.

Claims 1-3 and 7 are rejected under 35 U.S.C. §102(b) as anticipated by Heath et al. (US 4,901,234). Claims 4-6 and 8 are rejected under 35 U.S.C. §103(a) as unpatentable over Heath et al. in view of Bowes et al. (US 5,655,151). The rejections are respectfully traversed.

Heath discloses a computer system in which peripherals greater in number than the number of DMA channels provided in the system can all have DMA access. Some of the DMA channels are dedicated to certain ones of the peripherals, while others, termed "programmable" DMA channels, are shared by remaining ones of the peripherals (Abstract). A DMA controller 12 is coupled to a system bus 26 and a family bus 25 (Fig. 1). The details of DMA controller 12 are shown in Fig. 6.

Applicant's claim 1 is directed to a DMA controller comprising at least one peripheral DMA channel for handling DMA transfers on a peripheral access bus, at least one memory DMA stream, including a memory destination channel and a memory source channel, for handling DMA transfers on first and second memory access buses, first and second address computation units for computing updated memory addresses for DMA transfers, first and second memory pipelines for supplying memory addesses to the first and second memory access buses, respectively, and for transferring data on the first and second memory access buses, and a multiplexer configured to

supply first and second current memory addresses to selected ones of the first and second memory pipelines in response to a control signal.

Heath discloses a DMA controller having a peripheral bus 25 connected to a plurality of peripherals and a system bus connected to main memory 15. Thus, Heath may be considered as disclosing a DMA controller connected to a peripheral bus and to a single memory bus. However, Heath contains no disclosure or suggestion of a DMA controller having a memory destination channel and a memory source channel for handling DMA transfers on first and second memory access buses, as required by claim 1. Further, Heath contains no disclosure or suggestion of a DMA controller connected to a peripheral access bus and to first and second memory access buses, as required by claim 1.

The Examiner asserts that the connection between DMA controller 12 and main memory 15 and also between DMA controller 12 and auxiliary memory 17 reads on the memory destination channel and the memory source channel for handling DMA transfers on first and second memory buses. However, the family bus 25 of Heath cannot read on both the peripheral access bus and one of the memory access buses recited by claim 1.

The Examiner asserts that elements 52 in Fig. 6 contain first and second address computation units. However, Heath contains no disclosure or suggestion that the DMA controllers 52 shown in Fig. 6 contain address computation units.

The Examiner asserts that system bus 26 and family bus 25 shown in Fig. 1 of Heath read on the first and second memory pipelines for supplying memory addresses to the first and second memory access buses. However, the family bus 25 of Heath cannot read on both the peripheral access bus and one of the memory access buses recited by claim 1. Further, a memory pipeline is very different from a memory bus.

In addition, the cited passages of Heath contain no teaching or suggestion of a multiplexer configured to supply first and second current memory addresses to selected ones of the

first and second memory pipelines, as required by claim 1. In fact, Heath contains no disclosure of the structure of DMA controllers 52 shown in Fig. 6 and therefore cannot anticipate Applicant's claim 1. For these reasons, Heath does not disclose or suggest a DMA controller as defined by claim 1, and withdrawal of the rejection is respectfully requested.

Claims 2-8 and 25-27 depend from claim 1 and are patentable over the cited references for at least the same reasons as claim 1.

Based upon the above discussion, claims 1-8 and 25-27 are in condition for allowance.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

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Respectfully submitted,

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